CVAX and Rigel:
The Development Process

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Introduction

- CVAX is the second generation single chip VAX microprocessor
  - 2.5X to 3.5X 11/780 performance
  - CMOS-1 (2u) process technology
  - 175,000 transistor sites in CPU
  - PG in Q1 FY87, system FRS in Q1 FY88
- Rigel is the third generation single chip VAX microprocessor
  - 6X to 8X 11/780 performance
  - CMOS-2 (1.5u) process technology
  - 325,000 transistor sites in CPU
  - PG in Q1 FY88, system FRS in Q2 FY89
- CVAX and Rigel use an evolutionary extension of the full custom design methodology employed in MicroVAX
  - Structured design style
  - Floorplan (physical partitioning) driven
  - Multi-level hierarchical simulation
  - Fully hand-crafted layout
  - Logical and physical verification

Overall Design Process

- System performance model
  - Functionally crude but accurate models of system components
  - Trace driven simulation of large programs
  - Full modelling of TB, cache, I/O, multiprocessor effects
  - Used for high level design tradeoffs (TB and cache structures, bus protocols, chip partitioning)
  - Unique PASCAL program per system
- Chip (set) external specification
  - Defines external interface and protocols
  - Reviewed by system groups and customers
  - Used by customers as basis for system designs
- Chip (set) design specification
  - Defines internal blocks, functions, and interfaces
  - Reviewed by design team and external reviewers
  - Used by designers as highest level reference

Overall Design Process, continued

- Chip (set) behavioral model
  - Starts as RTL transcription of design specification
  - Equation level descriptions of all logic blocks
  - Used by designers to guide/verify logic design
  - Used by microcoders to debug/verify microcode
  - Used by logic modellers as shell for logic simulation
  - Used by test developers to debug/verify tests
  - Incrementally updated to greater accuracy as design progresses
- Physical partitioning (floorplanning)
  - Based on behavioral model
  - Detailed area, routing estimates for all major sections
  - Establishes layout feasibility, guides layout
- Logic design (unsized schematics)
  - Based on behavioral model
  - Entered via terminal/workstation, maintained online
  - Verified with standalone or mixed mode switch level simulation
  - Logic simulation expands from schematics to sections to entire chip

Overall Design Process, continued

- Circuit design (sized schematics)
  - Based on unsized schematics
  - Done by table lookup from design guides, or by iterative analysis
  - Verified with circuit level simulator at small schematic level
- Layout design (physical data base)
  - Based on sized schematics
  - Done by skilled professionals online with dedicated workstations
  - Verified against physical design rules and schematics
- Final design checks
  - Power/ground grid, electromigration analysis
  - Coupling, dynamic node noise analysis
  - Whole chip layout verification
  - Whole chip timing verification (still very crude)
  - Resimulation of critical paths with physically correct parameters

Overall Design Process, continued

- Pattern generation – PG
  - Direct transcription of online layout data base to masks
- Debug
  - Component level verification with test vectors
  - Subsystem level verification with macrocode programs
  - System level verification with VMS, AXE, Ultrix
  - Problem isolation in logic, circuits, manufacturing
- Manufacturing introduction
  - Reliability demonstration
  - Process tolerance demonstration (characterization)
  - Risk production and prototype approval
  - Limited Release
- Volume production
  - Yield demonstration
  - Test time and coverage demonstration
  - Yield improvement plan
  - Field feedback
  - Production Release

High Level Specification, Verification

- Specification
  - Performance model
  - Written specifications
  - Behavioral model (functional level)
- Verification
  - System level traces for performance checking
  - Behavioral execution with microcode
  - Macro diagnostics and DVTs (EVKAA, HCORE, small benchmarks)
  - AXE ($>$ 150k cases per instruction group)
  - Bootstrapping of VAXELN, VMB

Low Level Specification, Verification

- Specification
  - Iterated behavioral model (accurate to schematic level)
  - Sized schematic set
- Verification
  - Regression testing on behavioral model as updated
  - Standalone and mixed mode logic simulation from schematic up through entire chip
  - Design rule and interconnect verification of layout from individual cell up through entire chip
  - Back end checks of whole chip effects (coupling, noise, power, electromigration, etc)
  - Whole chip timing verification (for gross timing errors)
  - Resimulation of critical paths with physically correct parameters

Tools

Activity	CAD Tool
data management	CHAS or KATIE
behavioral modelling	DECSIM
logic entry	Quickdraw
logic verification	DECSIM MOS
circuit sizing	SPICE, tables
physical design	GDS-II or MEGAN
physical verification	DRC
phys reconciliation	IV
back end checks	XREF
timing verification	TV
pattern generation	MDP

Except for GDS-II (which is being phased out), DRC, and MDP, all of these tools were developed by DEC. All of these tools are supported by the SEG CAD group.

System Level Processes

- Chip behavioral model is component to larger system level model
- Systems groups build whole system behavioral model for functional verification, test pattern generation
- First system user is tightly coupled to chip development team (colocation, joint debugging)
- System level functional checkout is prerequisite to chip release

Libraries

- Process models
  - Detailed process models, based on extracted data, for circuit analysis using SPICE
  - Crude process models, abstracted from detailed model, for fast simulation of circuit effects in logic simulator
  - Reliability models for power, electromigration analyses
- Circuit libraries
  - Reusable components (I/O buffers, latches, etc) developed by design teams
  - High performance memory predesigns (ROM, RAM, CAM) developed by SEG/AD Memory design team
  - Design is full custom, all other circuits are unique to each chip

Testing Goals

- Testing
  - Probe (initial wafer sort) test time $<$ 20 seconds/die
  - Final (die sort) test time $<$ 10 seconds/die
  - $>$ 99 percent correlation to next higher level of assembly
- Yield
  - Probe test yield goal is a direct function of die size and transistor count
  - Final test yield is expected to start at 50 percent and rise steadily thereafter
- Reliability
  - Set by DEC standard for IC components
  - Operating temperature range of 0 C - 70 C
  - $>$ 1,000,000 MTBF
- Repair – not applicable. Failing parts are put on the cover of the Annual Report.

Test Strategy

- Engineering test strategy
  - Component level DVTs runnable on behavioral simulator, logic simulator, real chip
  - 100 percent nodal coverage, full functional coverage
  - Macro DVTs and diagnostics runnable on behavioral simulator, logic simulator, real chip
  - Bench tester with microprober, test generator, and logic analyzer, linked to chip models, for debug
  - ELN, Ultrix, VMS debug as part of chip checkout
- Manufacturing test strategy
  - Design for test features inbuilt in chips
  - 100 percent nodal coverage correlated to functional coverage
  - Demonstration of tolerance to process variations prior to release
  - Demonstration of reliability prior to release
  - High volume specialized production testers
  - Initial screen at wafer level to catch functional failures
  - Final screen at die level to catch parametric failures
  - Multiple speed bins from day 1
  - Statistical feedback from test results to design team
- Field Service test strategy – system level issue.

Intermittent Failures

- Chip failure mechanisms are different from system failure mechanisms
  - Alpha particle upset of dynamic memory cells
  - Burst bond wire
  - Electromigration
  - Hot electrons

  In particular, transistors do not suddenly appear or disappear (eg, a ROM will not change its contents)
- Intermittent failure techniques are tailored to failure mechanisms
  - Minimized use of dynamic latches outside memory arrays
  - Parity protection on dynamic memory arrays
  - Parity protection on data busses
  - Test of microprocessor critical paths as part of board self test

  Note that the intermittent failures in a single board CPU are very different, in type and number, from a multi board system

Test Development/Techniques

- Component level tests are developed by engineering
  - DVTs driven from specs for functional verification
  - Vectors driven from schematics for nodal verification
  - All tests are hand coded and debugged on the behavioral and/or logic simulators
  - Test vectors are formally qualified as part of release process
- Parametric tests are developed by manufacturing
  - Control programs for wafer and die sort
  - AC and DC parametric tests for die sort
  - AC characterization tests for process tolerance demonstration
  - All programs are hand coded and debugged on the actual test hardware
  - Test programs are formally qualified as part of release process
- System level tests are standard from chip to chip (EVKAA, HCORE, AXE, VMS, ELN, ULTRIX)

New Technologies

- Process Technology
  - CMOS-1 (2u) and CMOS-2 (1.5u) processes
  - Developed by LSI Mfg/Adv Semi Development
  - Supported by LSI Mfg/Adv Mfg Engineering
  - CAD support jointly by LSI Mfg/ASD and SEG/CAD
  - Process strategy, with CAD support, is joint partnership of engineering and manufacturing
- Packaging Technology
  - Surface mount 1 (50 mil) and 2 (25 mil) techology
  - Surface mounted ceramic packages (44, 68, 84, 132, 164, 196 pins)
  - Tape area bonding (TAB) for $>$ 132 pin packages
  - Packaging strategy, with CAD support, is joint partnership of LSI Mfg and P/DS
- Test Technology
  - Design for test hooks in chips
  - New high performance testers (Sentry 21, Takeda-Reiken)

Data Management

- Entire chip data base managed by central data manager and tool interface
  - CHAS – first generation, DBMS based, not suited to distributed design environment
  - KATIE – current product, flexible data manager, suitable for operation in both clusters and workstations
  - KATIE not only manages data but provides flexible and user-invisible methods for integrating new tools and special procedures
- Data archiving
  - Online data bases are backed up by SEG Computer Resources using both disks and tapes
  - Full tape backups are made at PG of each pass
  - All data bases for released chips are maintained by Hudson Document Control
  - Data bases are archived with current tool revisions

Data Base Contents

- Specifications
  - Engineering (user) specification
  - Design specification
- Behavioral model and documentation
- Microcode and documentation
- Sized schematics (wirelists, logic simulation model are automatically derived from the schematics)
- Complete layout
- Package specifications and packaging procedures
- Checkout software and procedures
  - Component level DVTs and test vectors
  - Wafer sort, die sort, and characterization programs
  - Macrocode DVTs and diagnostics
- Selected verification results (final DRC, IV, simulations)
- CAD and design tools, both generic and special

To build the chip, Manufacturing requires, in addition, the process recipe, which is archived on a per process rather than a per chip basis

Revision Control

- Revision sources:
  - Functional errors (bugs found in use)
  - Manufacturing problems (tolerance to process variation)
- Functional errors are disastrous, as there is no effective ECO method other than total replacement. The chip must be right when released to production. This is why full system test is an essential prerequisite to production release. Areas of particular concern:
  - Power up/power failure
  - Interrupts
  - DMA
- Manufacturing problems
  - Chip is followed by full time manufacturing engineer both before and after production release
  - Statistics on yield vs process variations are gathered continuously
  - Field returns are also monitored to gather failure data
  - Production problems are first screened out, then tweaked out by targetting the process, and then designed out by the chip team

CVAX/CFPA Resources

- Engineering manpower = $10M
- Engineering capital
  - 3 dedicated 785s, 2 shared 86XXs
  - 4 uVAX workstations
  - 9 Calma workstations
  - 2 bench testers
  - Terminal per team member, office and home
  - Multiple system prototypes
- Test manpower = $.6
- There are no special test capital investments for this project
- Manufacturing manpower = $.9M
- There are no special manufacturing capital investments for this project, beyond the general investment in CMOS-1 manufacturing

Rigel Resources

- Engineering manpower = $14M
- Engineering capital
  - 1 dedicated 8800, 1 dedicated 86XX
  - 20 uVAX workstations
  - 2 bench testers
  - 1 shared SEM based debug system
  - Terminal per team member, office and home
  - Multiple system prototypes
- Test manpower = $.9M
- There are no special test capital investments for this project
- Manufacturing manpower = $.1.6M
- Manufacturing capital
  - Rigel is dependent on success of, and capital investment in, TAB technology program
  - Rigel is also dependent on the success of, and capital investment in, the CMOS-2 program

Integration

- Engineering, Test, Manufacturing function as one team
  - Test engineer and manufacturing (product) engineer join during design phase, live with design team
  - Engineering fields support team to work with test and manufacturing for full year following Limited Release
  - Jointly agreed goals on yield, reliability, test correlation, etc provide joint success metrics for all groups
- Engineering, Test, Manufacturing function reside at same site
  - Increases bandwidth of communication
  - Facilitates joint problem solving and closure
- Engineering, Test, Manufacturing use same CAD tools and models
  - Behavioral model ties together microcode, functional verification, test patterns
  - Circuit models used for design development and manufacturing problem analysis
  - Manufacturing problem data base maintained online

The Bottom Line

The basis for success is commitment to, and achievement of, excellence in design, implementation, and follow up. Good processes are no substitute for good people.